former and increases their concentration in the latter. Owing to this, the hole concentration along an axis perpendicular to surface is trapezioidal in zero approximation. It puts certain restrictions both on the designing parameters of BSIT and on designing of circuits in which these transistors are applied. Algorithm of control of the offered transistor (offered) under typical circumstances is more complicated than (that) algorithm of control of the transistor described above ([1]) [3]. Let potentials of gates equal potentials of source and drain accordingly. Channels of transistor are closed. Flowing to drain electrode electrons can cause emission of holes from gate, disposed near the drain. Holes flow to gate, disposed near the source. Part of holes flow in channel and causes flowing of electrons to drain. So, there is positive feedback in the transistor. To preserve feedback it is necessary to provide so as electrons flow to drain free. It depends both on a control circuit and on a construction of the transistor. Control circuit is out the application. The construction of the transistor provides way for electrons to drain through thick channel, which is opened at potential of gate equals zero relatively the drain. Potential of drain of thick channel have to be positive or zero or little negative relatively potential of drain. Potential of source of thick channel have to be positive so as channel is closed.

C4

(To achieve optimum characteristics three rather than two different levels of voltages should be applied to the transistor gates. One of (the) voltages to the gate is about zero relatively to the nearby source, with the transistor channel closed, gate extracts holes, while the voltage applied to the gate near the drain should be about 0.4 V with the channel slightly open and the gate emit (ting) very low hole current to the channel and the lightly doped area).

When changing polarity of the voltage is applied, the source and the drain change places, and (the voltages to the gates) potentials of thick channels should be changed accodingly so as transistor is to remain closed. In this case the transistor can maintain voltages up to several kilovolt depending on parameters of the lightly doped area. Another voltage on (the) gates is about 0.8 V relatively of the (sourse) source and the drain which are nearby. It provides the opening of (the) channels and hole emission to the lightly doped area. The emission of holes to the lightly doped area is followed by electrons from the transistor source which makes the hole concentration and electron concentration (practically) the same in the zero approximation and may reach the magnitude of 10.sup.17÷ 10.sup.18 cm.sup.-3; resistance of the transistor drops abruptly (sharply) due to conductivity modulation and the voltage between the drain and the source of the transistor does not exceed 0.5 V at current density≈1000 a cm.sup.-2. (The level of 0.4 V can be substituted by) There is a smoothly lowering voltage on the gate which is near the source of the transistor during the switching of the transistor from on-condition to off-condition, owing to extraction.

"paragraph 0012". The control signals on (the) gates of the transistor should depend both on a polarity of the supply voltage (as a rule, it is alternating voltage with the frequency 50-60 Hz) and on the voltage applied (supplied) at the moment to the transistor; (to do so, it is desirable to introduce to the transistor structure) two normally-on channels (transistors) with small (saturation) current have been introduced to the transistor structure to help to (fix) determine a value and the polarity of the voltage on the transistor at (that) the moment. Signals from these channels (transistors) are transmitted to the control circuit which produces control signals to (the) gates. Besides, potentials and currents applied to electrodes of normally-on channels with control circuit change operating duty of the transistor and the thyristor themselves.

C5

"paragraph 0015". Apart from the main purpose of application, that is using the (transistor) device as a completely controlable power bidirectional key, (similar structure) device can be used (for other purposes; to achieve these purposes, both the control of emission and of extraction of holes into lightly doped area are used, as well as current feedback for the control of emission (for example, latch when manufacturing a switchboard)) as thyristor. Current feedback

C6

C6 provides the hole emission from gate, which is near drain of device, if the channel is lightly doped one and control circuit provides its.

"paragraph 0019". Inventions is explained with (three) five drawings.

"paragraph 0020" is canceled.

"between paragraph 0020 and paragraph 0021" Fig.4 represents a power normally-off transistor-thyristor structure with two lowpower normally-on channels.

C7 Fig.6 represents a power normally-off transistor structure with two lowpower normally-on channels disposed in epitaxial layers.

"paragraph 0021" is canceled.

"paragraph 0022" FIG. (3) 8 represents a symbolic image offered of the power normally-

C8 off transistor with two lowpower normally-on channels (transistors).

"paragraph 0023" is canceled.

"between paragraph 0023 and 0024" The bipolar static induction transistor-thyristor fig.4 comprises lightly doped n-type substrate 28, gates 29, gate electrodes 30, thick channels 31, thick channel electrodes (n.sup.+-type polysilicon) 32, source and drain 33, ordinary channels 34, source and drain electrodes (n.sup.+-type polysilicon) 35, source and drain contacts 36, thick

C9 channel contacts 37.
The bipolar static induction transistor fig.6 comprises lightly doped n-type substrate 47, epitaxial layers 48, gates 49, gate electrodes 50, thick channels 51, thick channel electrodes (n.sup.+-type polysilicon) 52, thick channel contacts 53, ordinary channels 54, source and drain 55, source and drain electrodes (n.sup.+-type polysilicon) 56, source and drain contacts 57, isolation 58.

"paragraph 0024" is canceled.

"paragraph 0025". Symbolic image of power normally-off transistor with two lowpower

C10 normally-on channels (transistors) comprises gates (12, 13) 63,64; drains (sources) of lowpower channels (transistors) (14,17) 65,68; drains (sources) of a power transistor (15,16) 66,67.

"paragraph 0026". The offered transistor (offered) can be named "symmetric channel

C11 (tetrod) gecsod" or "conductivity modulation type simmetric field effect transistor".

AUTHOR: 01.23.2003 EDLIN S.D.

References

1.Aoki et al. Static induction type semiconductor device. U.S.Patent №4994870.H01L 29/78.H01L 29/72.H01L 29/80.Priority Apr.20.1988.

2.Edlin S.D. JFET transistor and method for manufacturing the same. R.F.Patent №2102818.H01L 29/80.Priority Apr.15.1992.

3.Edlin S.D. The application for issue of the patent of RF №2000100080. A bipolar static induction transistor.H01L 29/06.Priority 01.05.2000.

4.Smoliansky B.A. et al.Author's certificate USSR №736807.H01L 29/70. Priority 01.22.1979.